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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,183	07/30/2001	Daniel B. D'Souza	00-464	2696

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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/918,183	Applicant(s) D'SOUZA, DANIEL B.	
	Examiner Paresh Patel	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 05/26/2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 10-20 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 05/20/2003 have been fully considered but they are not persuasive.

In combination DeHaven et al. and D'Souza et al. discloses all the elements of claimed invention including applicant's argument where applicant argues that neither one of the cited references discloses or suggests providing a plurality of DRAM dies on the wafer and conductive connection (inherent to testing because conductive connection is needed to test the ICs of product wafer) providing that said DRAM's **can be** burned-in on the wafer.

Applicant argues that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, DeHaven suggests testing of product (ICs on wafer) wafer with testing wafer (CDW). CDW also performs burn-in operations on the ICs of product wafer. At lines 65-67 of column 4 and at lines1-7 of column 5, DeHaven discloses **ICs of the product wafer are one or more of** microprocessors, microcontrollers, digital signal processors, analog filters, A/D or D/A

converters, memory circuits, EEPROMs, EPROMs, **DRAMs,** SRAMs ...or any other compatible IC device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over D'Souza et al. (US 5396170) in view of DeHaven et al. (US 6411116).

Regarding claim 1, D'Souza et al. (hereinafter D'Souza) in fig. 9 discloses: a plurality of DRAM dies [908a-908d], wherein each DRAM die has a test data in pad [contact terminal of TDI at 908a] and a test data out pad [contact terminal of TDO at 908a]; and

conductive connections [electrical connection between TDO of 908a and TDI of 908b] interconnecting the test data out and test data in pads of the DRAM dies.

D'Souza does not disclose a plurality of DRAM dies **on the wafer** and conductive connection providing that said **DRAM's can be burned-in on the wafer**. Rather, D'Souza discloses DRAM dies are mounted on a printed circuit board [902] of probe card [900]. Here the DRAM dies are used to conduct test on DUT [952 of fig. 10].

DeHaven et al. (hereinafter DeHaven) in fig. 3-5 discloses a plurality of DRAM dies [34 and see lines 53-59 of column 3] **on the wafer** [16] and said conductive

connection providing that said **DRAM's can be burned-in on the wafer** [lines 35-44 of column 3]. It would have been obvious to a person having ordinary skill in the art at the time the invention to use connection of DRAM dies of D'Souza with the wafer as taught by DeHaven, in order to study reliability and functionality of individual dies on a wafer before singulating and shipping, because individual testing of DUT (packaged chip or die) is costly if failure rate is higher during manufacturing process (also see lines 44-67 of column 2).

Regarding claim 2, D'Souza discloses: DRAM dies are IEEE1149.1 compliant [lines 49-52 of column 13], and include Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Set (TMS) pads [see fig. 9].

Regarding claim 3, D'Souza discloses: TDO pad of each DRAM die is connected to the TDI pad of next DRAM die [see fig. 9].

Regarding claims 4-5, D'Souza discloses: TMS and TCK pads of the DRAM dies are connected in parallel [see fig. 9] via metal lines [conductive lines connecting TMS and TCK to 908a-d] running along a scribe area [area of 900].

Regarding claim 6, D'Souza discloses the DRAM dies are arranged in rows [see fig. 9], and each DRAM die in a given row is daisy chained to the next DRAM die in the raw [fig. 9].

Regarding claims 7-8, D'Souza discloses metal line to connect two DRAM dies [conductive lines connecting TDO and TDI to 908a-d]. DeHaven and D'Souza discloses claimed invention except for **last DRAM die in raw is daisy chained to the first DRAM die in the next raw**. It would have been an obvious matter of design choice to

connect last DRAM die in raw is daisy chained to the first DRAM die in the next raw, since applicant has not disclosed that last DRAM die in raw is daisy chained to the first DRAM die in the next raw solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with combination of DeHaven and D'Souza.

Regarding claims 9, DeHaven discloses the DRAM dies on the wafer are connected to the power busses [26-28 of column 9].

Conclusion

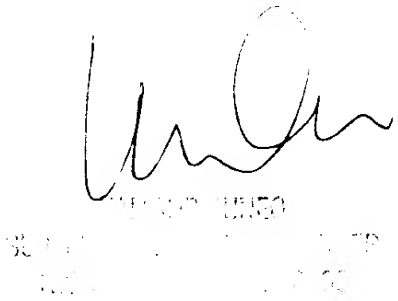
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Paresh Patel
July 24, 2003